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09/930,956	08/17/2001	Jun Koyama	12732-071001	1626

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EXAMINER	
SHENG, TOM V	

ART UNIT	PAPER NUMBER
2673	9

DATE MAILED: 10/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/930,956	KOYAMA ET AL.	
	Examiner	Art Unit	
	Tom V Sheng	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *23-49* is/are allowed.

6)☒ Claim(s) *1-22 and 50-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,8* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-53 in Paper No. 7 is acknowledged.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1-11 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-10 of copending Application No. 09/931061. Although the conflicting claims are not identical, they are not patentably distinct from each other because it would have been obvious for one of ordinary skill in the art at the time of the claimed invention that the use of both (volatile) and non-volatile memory circuits in a pixel are applicable to various kinds of

matrix displays and further applicable to a variety of electronic devices that utilizes a display.

Claims 12-22 are provisionally rejected over claims 11-20 of the copending application for the above same reason.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

4. Claims 23-35 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 21-32 of copending Application No. 09/931061. Although the conflicting claims are not identical, they are not patentably distinct from each other because even though claims 23-35 of the current application are directed to liquid crystal display and claims 21-32 of the copending application are directed to electro-luminescent display, the corresponding pixel-memory structure and writing/reading method are exactly the same, and it would have been obvious for one of ordinary skill in the art at the time the invention was made that the pixel-memory structure and functionality are factually independent from the display type.

Claims 36-49 are provisionally rejected over claims 33-45 of the copending application for the above same reason.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 4, 9-12, 15, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner (US Patent 6246386 B1) in view of Kobayashi (US Patent 4432610).

As for claims 1 and 12, Perner teaches a liquid crystal display device (figure 2) having a plurality of pixels (figure 7; matrix 174 of NxM pixels 176; column 11, lines 22-29), each of the plural pixels comprising a plurality of (n x m) memory circuits (each pixel of the LCD has eighteen dual port DRAM cells; column 5, lines 47-59). For Perner, n is 18 and m is 1.

Perner does not teach a plurality of (n x k) non-volatile memory circuits in addition to a plurality of memory circuits. Kobayashi teaches that when nonvolatile memory transistor is used in the pixel of a LCD device, the data stored would not be erased even in the case of a momentary power failure. See figure 2, individual pixel memory cell 12, and column 4, line 60 - column 5, line 12.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to incorporate a plurality of non-volatile memory circuits of Kobayashi with a plurality of memory circuits of Perner in a LCD device because of the benefit of maintaining a last picture being displayed before the device is either shutdown

due to a momentary power failure or unplugged from a power source for moving to a different location. For example, n = 18 and k =1 if only one non-erasable frame is desired.

As for claims 4 and 15, Perner's memory circuits are DRAM cells.

As for claims 9 and 20, Kobayashi teaches the forming of non-volatile memory transistors on a monocrystalline silicon substrate.

As for claims 10-11 and 21-22, LCD devices are well known to be incorporated in an electronic device such as television set, personal computer, portable terminal, video camera, and head mounted display.

7. Claims 2, 5, 13, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi as applied to claims 1 and 12 above, and further in view of Yamazaki et al. (US Patent 5699078).

As for claims 2, 5, 13, and 16, Perner teaches the use of DRAM for the memory circuits. Perner does not teach using SRAM for the memory circuits and EEPROM for the non-volatile memory circuits.

Yamazaki teaches the incorporation of a memory in which information on the characteristics of the pixels are stored, into a liquid crystal device. See column 2, lines 23-30. Moreover, Yamazaki teaches that volatile memories such as DRAM and SRAM, as well as non-volatile memories such as EEPROM and flash memories are suitable choices. See column 4, lines 36-40.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to incorporate SRAM of Yamazaki as the memory circuits and EEPROM of Yamazaki as the non-volatile memory circuits because they are all suitable choices in implementing the memories. Certainly, factors such as design complexity, sizes, and etc. would come into play.

8. Claims 3 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi as applied to claims 1 and 12 above, and further in view of Yamazaki et al. (US Patent 5349366).

As for claims 3 and 14, Perner teaches the use of DRAM for the memory circuits. Perner does not teach using FeRAM for the memory circuits.

Yamazaki teaches the incorporation of material such as ferroelectrics to function as memory.

It would have been obvious for one of ordinary skill in the art at the time the invention was made that the memory taught by Yamazaki can be applied for the memory circuits of Perner, because it would allow rewriting only specified pixels as taught by Yamazaki and would also simply constitute an alternative choice of memory component in the pixel. See Abstract and column 9, lines 40-55.

9. Claims 6 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi as applied to claims 1 and 12 above, and further in view of Parks (US Patent 5471225).

As for claims 6 and 17, Perner teaches a LCD device incorporating an array of memory circuits with each pixel. However, Perner does not teach that the memory circuits are formed on a glass substrate.

Parks teaches a LCD having a plurality of storage cells. Further, provided across a glass material are the storage cells comprising bit lines, word lines, display electrodes, pass-gate transistors, and latching circuits for storing video data.

It would have been obvious for one of ordinary skill in the art at the time the invention was made that glass substrate of Parks is a good insulator for laying the memory and driving circuits of an LCD display. Also, the transparent property of glass lends naturally to use with liquid crystal display, and thus accounts for the common usage.

10. Claims 7 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi as modified by Parks as applied to claims 1/12 and 6/17 above, and further in view of Fonash et al. (US Patent 5945866).

As or claims 7 and 18, Perner as modified teaches a LCD device having an array of memory circuits per pixel; wherein the memory circuits are formed on a glass substrate.

Perner as modified does not teach that a plastic substrate can be used also.

Fonash teaches that TFTs can be deposited on either glass or plastic substrate (figure 1). TFTs are transistor circuits used for driving as well as memory circuits of Perner as modified. See column 1, lines 44-52.

It would have been obvious for one of ordinary skill in the art at the time the invention was made that either substrate, glass or plastic of Fonash, can be used for manufacturing the circuits, which is readily recognized as an alternative material choice.

11. Claims 8 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Perner and Kobayashi as modified by Parks as applied to claims 1/12 and 6/17 above, and further in view of Johnson (US Patent 4752118).

As or claims 8 and 19, Perner as modified teaches a LCD device having an array of memory circuits per pixel; wherein the memory circuits are formed on a glass substrate.

Perner as modified does not teach that a stainless steel substrate can be used also.

Johnson teaches that amorphous integrated circuits can be deposited on either glass or stainless steel (column 1, line 22 - column 2, line 2). In the case of stainless steel, it should first be coated with a layer of insulating layer (column 8, line 61 - column 9, line 2).

It would have been obvious for one of ordinary skill in the art at the time the invention was made that either substrate, glass or stainless steel of Johnson, can be used for manufacturing the circuits, which is readily recognized as an alternative material choice.

12. Claims 50-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicants' admitted prior art in view of Perner (US Patent 6246386 B1).

As for claim 50, applicants' admitted art teaches a method of driving a liquid crystal display device using n (n is a natural number and satisfies 2 <= n) bit digital video signals to display an image (admitted art uses 3 bit digital gray scale per pixel), the liquid crystal display device including a source signal line driver circuit (figure 13, circuit 1301), a gate signal line driver circuit (circuit 1302), and a plurality of pixels (pixels as defined by intersections formed by the gate lines and signal lines),

wherein shift registers (figure 14, shift registers 1401) in the source signal line driver circuit output sampling pulses (sequentially generated by clock signals and start pulses), which are inputted to latch circuits (first latch circuits 1402 then second latch circuits 1403), which hold the digital video signals in response to the sampling pulses, the held digital video signals being written in a source signal line (digital video signals D/A converted to analog video signals and driven through signal lines to the pixels),

wherein gate signal line selecting pulses are outputted in the gate signal line driver circuit to select a gate signal line (inherent in active matrix LCD display).

Admitted Art does not teach wherein **one of the following** (a) through (e) is conducted in pixels in the row of the selected gate signal line out of the plural pixels:

(a) the n bit digital video signals inputted from the source signal line are written in memory circuits;

(b) the n bit digital video signals stored in the memory circuits are read;

(c) the n bit digital video signals inputted from the source signal line or the n bit

digital video signals stored in the memory circuits are written in non-volatile memory circuits;

(d) the n bit digital video signals stored in the non-volatile memory circuits are read; and

(e) the n bit digital video signals stored in the non-volatile memory circuits are written in the memory circuits.

On the other hand, Perner teaches driving a LCD display wherein each pixel has 18 x 1 (3 rows of 6 memory cells) memory circuits. In one instance (figure 8), pixel data is written one row at a time and in 3 times. This reads on **part (a)** where n = 18.

It would have been obvious for one of ordinary skill in the art at the time the invention was made to incorporate Perner's memory circuits into admitted art because of the enhancement in efficiency by reducing the need to access the external memory for video data.

As for claim 51, when a still image is displayed, it would be most efficient to just access the pixel memories for each display period.

As for claims 52-53, LCD devices are well known to be incorporated in an electronic device such as television set, personal computer, portable terminal, video camera, and head mounted display.

Allowable Subject Matter

13. Claims 23-49 are allowed.

14. The following is a statement of reasons for the indication of allowable subject matter: none of the prior arts of record teaches the recitations

"wherein each gate electrode of the n writing transistors is electrically connected to one of the n writing gate signal lines, with no two gate electrodes sharing the same writing gate signal line, wherein each input electrode of the n writing transistors is electrically connected to the source signal line, wherein each output electrode of the n writing transistors is electrically connected to one of m circuits out of the n x m memory circuits through one of n units out of the 2n memory circuit selecting units, each memory circuit selecting unit making selection for no more than one output electrode, wherein each output electrode of the n writing transistors is electrically connected to one of k circuits out of the n x k non-volatile memory circuits through one of n units out of the 2n non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one output electrode, wherein each gate electrode of the n reading transistors is electrically connected to one of the n reading gate signal lines, with no two gate electrodes sharing the same reading gate signal line, wherein each input electrode of the n reading transistors is electrically connected to one of m circuits out of the n x m memory circuits through one of n units out of the 2n memory circuit selecting units, each memory circuit selecting unit making selection for no more than one input electrode, wherein each input electrode of the n reading transistors is electrically connected to one of k circuits out of the n x k non-volatile memory circuits through one of n units of the 2n non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than

one input electrode, and wherein each output electrode of the n reading transistors is electrically connected to one of electrodes of the liquid crystal element" and remainder as cited in claim 23, and

"wherein each gate electrode of the n writing transistors is electrically connected to the writing gate signal line, wherein each input electrode of the n writing transistors is electrically connected to one of the n source signal lines, with no two input electrodes sharing the same source signal line, wherein each output electrode of the n writing transistors is electrically connected to one of m circuits out of the n x m memory circuits through one of n units out of the 2n memory circuit selecting units, each memory circuit selecting unit making selection for no more than one output electrode, wherein each output electrode of the n writing transistors is electrically connected to one of k circuits out of the n x k non-volatile memory circuits through one of n units out of the 2n non-volatile memory circuit selecting units, each non-volatile memory circuit selecting unit making selection for no more than one output electrode, wherein each gate electrode of the n reading transistors is electrically connected to one of the n reading gate signal lines, with no two gate electrodes sharing the same reading gate signal line, wherein each input electrode of the n reading transistors is electrically connected to one of m circuits out of the n x m memory circuits through one of n units out of the 2n memory circuit selecting units, each memory circuit selecting unit making selection for no more than one input electrode, wherein each input electrode of the n reading transistors is electrically connected to one of k circuits out of the n x k non-volatile memory circuits through one of n units out of the 2n non-volatile memory circuit selecting units, each

non-volatile memory circuit selecting unit making selection for no more than one input electrode, and wherein each output electrode of the n reading transistors is electrically connected to one of electrodes of the liquid crystal element" and remainder as cited in claim 36.

Claims 24-35 are dependent on claim 23 and claims 37-49 are dependent on claims 36.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tom V Sheng whose telephone number is (703) 305-6708. The examiner can normally be reached on 8:30am - 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on (703) 305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

TS
October 14, 2003